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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,649	03/29/2001	Hongjiang Song	INTL-0550-US (P11109)	5728

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TROP PRUNER & HU, PC
8554 KATY FREEWAY
SUITE 100
HOUSTON, TX 77024

EXAMINER

WARE, CICELY Q

ART UNIT	PAPER NUMBER
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2611

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

8

Office Action Summary	Application No. 09/821,649	Applicant(s) SONG, HONGJIANG	
	Examiner Cicely Ware	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 January 2006 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see REMARKS, filed 1/17/2006, with respect to the rejection(s) of claim(s) 1-9 under 35 USC 102(b) and claims 10-15 under 35 USC 103(a) and claims 16-23 under 35 USC 103(a) and claims 24-28 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Gunzelmann et al. (US Patent 6,532,255).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 24-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Gunzelmann et al. (US Patent 6,532,255).

(1) With regard to claim 1, Gunzelmann et al. discloses in (Fig. 7) a locked loop circuit (5, 6); and processor (2) coupled to the locked loop circuit (2, 5, 6) to control the

locked loop circuit (Δ_1 , 5, Δ_2 , 6) and perform at least one other function in the system (3) not related to the control of the locked loop circuit.

(2) With regard to claim 2, claim 2 inherits all the limitations of claim 1.

Gunzelmann et al. further discloses in (Fig. 7) wherein the locked loop circuit comprises a delay locked loop circuit (5, 6).

(3) With regard to claim 24, Gunzelmann et al. discloses in (Fig. 7) an article comprising a computer accessible storage medium storing instructions (2) to, when executed cause a processor (2) to: receive indication of phase difference from a locked loop circuit (5, T1)) and control the locked loop circuit ($(\Delta_1$, 5, Δ_2 , 6)), wherein the processor performs at least one other function (2, 3, T₀) not related to the control of the locked loop circuit.

Gunzelmann et al. does not explicitly disclose a storage medium. It is well known in the art that a storage medium or memory is inherent to a microprocessor for storing instructions.

(4) With regard to claim 25, claim 25 inherits all the limitations of claim 23.

Gunzelmann et al. further discloses wherein the locked loop circuit comprises a delay locked loop circuit (Fig. 7 (5, 6)).

(5) With regard to claim 26, claim 26 inherits all the limitations of claim 24.

Gunzelmann et al. further discloses (Fig. 7) the storage medium storing instructions to cause the processor (2) to use the interface to receive the indication of the phase difference (5, 6, 2, T₁, T₂).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gunzelmann et al. (US Patent 6,532,255), as applied to claim 1, in view of Leonida (US Patent 5353025).

With regard to claim 3, claim 3 inherits all the limitations of claim 1. However Gunzelmann et al. does not disclose wherein the locked loop circuit comprises an interface accessible by the processor.

However Leonida further discloses in wherein the locked loop circuit comprises an interface accessible by the processor (Fig. 2 (116, 162, 118), Fig. 3 (118, 162, 182, 233)) (col. 5, lines 66-68 – col. 6, lines 3-8, col. 7, lines 65-68 – col. 8, lines 1-2).

Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. to incorporate wherein the locked loop circuit comprises an interface accessible by the processor in order to provide a variable delay with respect to the start of the circuit board operation (Leonida, col. 6, lines 53-59).

6. Claims 4-6, 8, 9, 12-14, 18-21, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunzelmann et al. (US Patent 6,532,255) in view of Leonida (US

Patent 5353025), as applied to claims 1 and 3 in view of Silvestri (US Patent Application 2002/0130691 A1).

(1) With regard to claim 4, claim 4 inherits all the limitations of claim 3. However Gunzelmann et al. in combination with Leonida does not disclose wherein the interface indicates a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit.

However Silvestri discloses in (Fig. 2 (54)) wherein the interface indicates a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit (Fig. 3, pg. 3, col. 2, lines 22-49).

Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. in combination with Leonida in view of Silvestri to incorporate wherein the interface indicates a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit in order to provide a memory device having a circuit which dynamically locks a DLL in a minimum number of cycles, which would provide a locking method and apparatus which coincides with the ever-increasing speed of microprocessing and memory access (Silvestri, Pg. 1, col. 2, lines 46-50).

(2) With regard to claim 5, claim 5 inherits all the limitations of claim 3. Silvestri further discloses in (Fig. 1) wherein the system comprises a computer system (26) having a system memory (Fig. 2 (38)) and the interface (Fig. 2 (12)) is addressable (Fig. 2 (34)) in a range of addresses used to access the system memory (Pg. 2, col. 2, lines 5-24, pg. 3, col. 1, lines 6-41).

(3) With regard to claim 6, claim 6 inherits all the limitations of claim 3. Silvestri further discloses in (Fig. 2 (54, 12), Fig. 3 (62)) wherein the interface indicates storage accessible by the processor to store an indication of a delay used by the locked loop circuit (Pg. 3, col. 2, lines 51-67).

(4) With regard to claim 8, claim 8 inherits all the limitations of claim 1. Silvestri further discloses in (Fig. 1 (12), Fig. 2 (12)) wherein the processor comprises a microprocessor (Pg. 2, col. 1, lines 34-41).

(5) With regard to claim 9, claim 9 inherits all the limitations of claim 1. Silvestri further discloses a system memory storing a program, wherein the processor executes the program to perform said other function (Pg. 2, col. 2, lines 5-24).

(6) With regard to claim 12, claim 12 inherits all the limitations of claim 10. Silvestri further discloses in wherein the interface indicates a phase difference between an incoming clock signal to the locked loop circuit and another signal generated by the locked loop circuit (Pg. 3, col. 2, lines 22-49).

(7) With regard to claim 13, claim 13 inherits all the limitations of claim 10 above. Silvestri further discloses in (Fig. 1) wherein the system comprises a computer system (26) having a system memory (Fig. 2 (38)) and the interface (Fig. 2 (12)) is addressable (Fig. 2 (34)) in a range of addresses used to access the system memory (Pg. 2, col. 2, lines 5-24, pg. 3, col. 1, lines 6-41).

(8) With regard to claim 14, claim 14 inherits all the limitations of claim 10. Silvestri further discloses wherein the interface includes storage accessible by the

processor to store an indication of a delay applied by the locked loop circuit to the input clock signal (Fig. 2 (54, 12), Fig. 3 (56, 58)).

(9) With regard to claim 18, claim 18 inherits all the limitations of claim 16.

Silvestri further discloses in (Fig. 2 (30)) performing at least one of read and write operations to the interface to control the locked loop circuit (Pg. 3, col. 1, lines 51-61, col. 2, lines 10-20).

(10) With regard to claim 19, claim 19 inherits all the limitations of claims 16 and 4.

(11) With regard to claim 20, claim 20 inherits all the limitations of claims 16 and 5.

(12) With regard to claim 21, claim 21 inherits all the limitations of claims 16 and 6.

(13) With regard to claim 23, claim 23 inherits all the limitations of claims 16 and 8.

7. Claims 7 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunzelmann et al. (US Patent 6,532,255) in view of Leonida (US Patent 5353025), in view of Silvestri (US Patent Application 2002/0130691 A1), as applied to claims 3 and 24 in further view of Dvorak et al. (US Patent 6,535,989).

(1) With regard to claim 7, claim 7 inherits all the limitations of claim 3.

Gunzelmann et al. in combination with Leonida in combination with Silvestri disclose all

the limitations of claim 3. However Gunzelmann et al. in combination with Leonida in combination with Silvestri do not disclose wherein the interface includes storage accessible by the processor to store an indication of a selection of one or more of a plurality of output clock signals furnished by the locked loop circuit.

However Dvorak et al. discloses in (Fig. 3 (500)) wherein the interface includes storage accessible by the processor (Fig. 5 (500, 515)) to store an indication of a selection (505) of one or more of a plurality of output clock signals furnished by the locked loop circuit (abstract, col. 1, lines 15-26, 57-60, col. 4, lines 10-35, col. 6, lines 43-48).

Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. in combination with Leonida in combination with Silvestri in view of Dvorak et al. to incorporate wherein the interface includes storage accessible by the processor to store an indication of a selection of one or more of a plurality of output clock signals furnished by the locked loop circuit in order to provide a PLL that can handle variable core-bus clock frequency ratios and not have to re-lock every time the ratio changes (Dvorak, col. 2, lines 19-26).

(2) With regard to claim 28, claim 28 inherits all the limitations of claim 24. Dvorak et al. further discloses in (Fig. 3 (500)) wherein the interface includes storage accessible by the processor (Fig. 5 (500, 515)) to store an indication of a selection (505) of one or more of a plurality of output clock signals furnished by the locked loop circuit (abstract, col. 1, lines 15-26, 57-60, col. 4, lines 17-35, col. 6, lines 43-48).

8. Claims 10, 11, 15, 16, 17, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dvorak et al. (US Patent 6,535,989) in view of Gunzelmann et al. (US Patent 6,532,255).

(1) With regard to claim 10, Dvorak et al. discloses a locked loop circuit comprising (Fig. 3, Fig. 4): a delay line (305-(1-8)) to receive an input clock signal and furnish an output clock signal; a phase detector (310) to indicate a phase difference between the input clock signal and the output clock signal (col. 1, lines 24-61, col. 3, lines 57-62, col. 4, lines 5-12).

However Dvorak does not disclose an interface accessible by a processor to control the locked loop circuit to adjust a timing between the input clock signal and the output clock signal based on the indicated phase difference.

However Gunzelmann et al. discloses in (Fig. 1) an interface (107) accessible by a processor (Fig. 7 (2, 5, 6)) to control the locked loop circuit to adjust a timing between the input clock signal and the output clock signal based on the indicated phase difference (col. 6, lines 32-65).

Therefore it would have been obvious to one of ordinary skill in the art to modify Dvorak et al. in view of Gunzelmann et al. to incorporate an interface accessible by a processor to control the locked loop circuit to adjust a timing between the input clock signal and the output clock signal in order to slave the phase angle of the locally produced spread sequence as accurately as possible to the directly received signal once the signal has been acquired (Gunzelmann et al., col. 2, lines 30-34).

(2) With regard to claim 11, claim 11 inherits all the limitations of claims 10. Gunzelmann et al. further discloses in (Fig. 7 (5, 6)) wherein the locked loop circuit comprises a delay locked loop circuit.

(3) With regard to claim 15, claim 15 inherits all the limitations of claims 10 and 7.

(4) With regard to claim 16, claim 16 inherits all the limitations of claims 1 and 3.

(5) With regard to claim 17, claim 17 inherits all the limitations of claims 16 and 2 above.

(6) With regard to claim 22, claim 22 inherits all the limitations of claims 16 and 7.

9. Claim 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunzelmann et al. (US patent 6532255) as applied to claim 24, in view of Silvestri (US Patent Application 2002/0130691).

With regard to claim 27, claim 27 inherits all the limitations of claim 24. However Gunzelmann et al. does not disclose the storage medium storing instructions to cause the processor to store an indication of a delay used by the locked loop circuit in an interface of the locked loop circuit.

However Silvestri discloses in (Fig. 1, Fig. 2) the storage medium storing instructions to cause the processor to store an indication of a delay used by the locked loop circuit in an interface of the locked loop circuit ((Fig. 2 (12, 34, 54), Pg. 2, col. 2, lines 5-24, pg. 3, col. 1, lines 6-41).

Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. in view of Silvestri to incorporate the storage medium storing instructions to cause the processor to store an indication of a delay used by the locked loop circuit in an interface of the locked loop circuit in order to provide a memory device having a circuit which dynamically locks a DLL in a minimum number of cycles, which would provide a locking method and apparatus which coincides with the ever-increasing speed of microprocessing and memory access (Silvestri, Pg. 1, col. 2, lines 46-50).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cicely Ware whose telephone number is 571-272-3047. The examiner can normally be reached on Monday – Friday, 8-5.

Art Unit: 2634

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Cicely Ware

cqw
March 20, 2006



KHAI TRAN
PRIMARY EXAMINER